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EXAMINER	
MARTINEZ, DAVID E	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,045	NODA, HIROYASU	
	Examiner	Art Unit	
	David E. Martinez	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *1 and 2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 12/1/03 has been considered by the examiner.

Claim Objections

Claims 1-2 are objected to because of the following informalities:

With regards to claim 1, it seems to contain several typos. In line 4 and line 8, the term "generator which, when," seems to read better when written "generator, which when". In line 6, the word --- a --- seems to be missing between "perform" and "writing". In line 11, the word --- a --- seems to be missing before the term "writing operation,".

With regards to claim 2, it also seems to contain several typos. In line 3, the term "generator which, when," seems to read better when written "generator, which when". In line 6, the term "having memory data" seems to be bad grammar. It would make better sense writing "has memory data". In line 7, the word --- a --- seems to be missing between "perform" and "reading operation". Also in line 7, the term "for read said memory" reads better "for reading said memory".

Due to the number of claim objections, the examiner has provided a number of examples of claim deficiencies, however, the list may not be all inclusive. Applicant should refer to these examples of deficiencies and should make all the necessary corrections to eliminate the problems and place the claims in a proper format. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 1, lines 1-2 are unclear as to what is connected with an external FIFO circuit, is it the extending circuit or an internal FIFO circuit? Also, line 7 refers to "outputting said input data into said external FIFO circuit". The outputting of input data seems to necessitate the receiving of data prior to the outputting of said data. This is an essential limitation that seems to be missing from the claim. Furthermore in lines 5-6, "judged that said external FIFO circuit can write data" is indefinite since it isn't as to where exactly can the external FIFO circuit can write data. Is it writing data to another adjacent circuit it is connected to or does it mean writing data to perhaps an internal buffer inside the external FIFO circuit itself? The same applies to lines 9-1, the term "judged that said external FIFO circuit can not write data" since it is unclear as to where the external FIFO circuit cannot write data to.

With regards to claim 2, lines 5-6 suffer from the same deficiencies as those of claim 1 above directed to the term "judged that said external FIFO circuit can write data" as it is unclear as to where exactly can the external FIFO circuit write data to. In lines 10-11, the term "said external FIFO circuit is judged being able to write data" also suffers from the same deficiencies.

With further regards to claim 2, in lines 12-13, the term "said data is received, outputs, prior to said input data, said memory data read out" is unclear and not understood. Is it outputting memory data prior to performing some kind of operation on input data? Is the input data being received or sent somewhere prior to outputting memory data?

With regards to claim 3, in lines 4-5, the term "the transmitting-receiving device using extending circuit for memory using the Extending circuit for memory" is unclear since it is not understood what it is trying to portray. Perhaps the applicant means "device using *the* extending circuit for memory ~~using the Extending circuit for memory~~ comprising:" ? In addition, several instances of "the extending circuit" and "the Extending circuit" (capitalized E) exist throughout the claim. It isn't clear if the lowercase and the capitalized extending circuit are referring to the same element. If they are, then consistency in the claim language is respectfully requested.

With regards to claim 4, lines 1-2 have the term "The transmitting-receiving device using extending circuit for memory using the Extending circuit for memory according to..." suffer from the same deficiencies as claim 3 above. Perhaps applicant meant "The transmitting-receiving device using *the* extending circuit for memory ~~using the Extending circuit for memory~~ according to...".

With further regards to claims 1 and 3, the word "effective" in claim 1 line 4 and claim 3 lines 12,16 and 20 is not understood. Is the word considered part of "an output data effective signal generator" as a name or does it mean it is effecting something else?

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,809,521 to Steinmetz et al. (hereinafter Steinmetz) in view of US Patent No. 5,956,492 to Jander et al. (hereinafter Jander).

With regards to claim 1, Steinmetz teaches an extending circuit [fig 1b element 12] for memory which has an internal FIFO circuit [fig 3b element 20] and is connected with an external FIFO circuit [fig 1b element 14], in order to extend memory capacity used for writing input data, comprising:

an output data effective signal generator [fig 1b element at output port labeled "nEmpty", fig 3b element 40] which, when, based on a status signal output [fig 1b "RFDAB" signal when asserted transmitted from element 14 to element 12, means element 14 is not full so there is room for data] from said external FIFO circuit [fig 1b element 14], judged that said external FIFO circuit can write data [element 14 uses the nFull port to send signal RFDAB to port "READ" of element 12 – column 4 lines 14-15 "ready for data status"], makes said external FIFO circuit perform writing operation, for outputting said input data into said external FIFO circuit [column 3 line 55 to column 4 line 1]; and

Steinmetz teaches all of the above limitations but is silent as to having an internal FIFO write enable generator which, when, based on said status signal output from said external FIFO circuit, judged that said external FIFO circuit can not write data, makes said internal FIFO circuit perform writing operation, for writing said input data into said internal FIFO circuit.

However, Jander teaches a FiFO [fig 1 element 100] having an internal FIFO write enable generator [fig 1 element 108], which, when, based on a status signal output from an external FIFO circuit [fig 1 element 104], judged that said external FIFO circuit can not write data [fig 2a step 204], makes said internal FIFO circuit perform writing operation, for writing said

input data into said internal FIFO circuit for the benefit of preventing data coherency by preventing new data from overwriting older data [column 4 lines 1-21].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Steinmetz and Jander to provide an internal FIFO write enable generator, which, when, based on a status signal output from an external FIFO circuit, judged that said external FIFO circuit can not write data, makes said internal FIFO circuit perform writing operation, for writing said input data into said internal FIFO circuit for the benefit of preventing data coherency by preventing new data from overwriting older data.

With regards to claim 2, Steinmetz teaches the extending circuit for memory according to claim 1, further comprising:

an internal FIFO read enable generator [fig 1b in element 12] which, when, based on said status signal [fig 1b element "RFDAB"] output from said external FIFO circuit [sent from element 14 port labeled "nFull"] and a status signal output from said internal FIFO circuit [fig 1b element "DAVAB" sent from element 12 from the port nEmpty to element 14], judged that said external FIFO circuit can write data and said internal FIFO circuit is having memory data, makes said internal FIFO circuit perform reading operation, for read said memory data out from said internal FIFO circuit and outputting said memory data to said external FIFO circuit [column 3 line 62 to column 4 line 1, and column 4 lines 11-17]; and

an output data generator which, when said external FIFO circuit [fig 1b element 14] is judged being able to write data [fig 1b element "RFDAB"]; and said internal FIFO circuit is judged having memory data [fig 1b element "DAVAB"]; and said input data is received [fig 1b element "RFDAB" is a not empty signal], outputs [fig 1b element 12 "DATAOUT", signal "DATAAB"], prior to said input data, said memory data read out from said internal FIFO circuit to said external FIFO circuit [column 3 line 62 to column 4 line 1, and column 4 lines 7-17].

Allowable Subject Matter

Claims 3-4 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record do not teach or fairly suggest a transmitting-receiving device using an extending circuit for memory having a first selector for enabling a transmission or reception signal, a second selector for enabling a status signal from either the transmission FIFO circuit or the reception FIFO circuit, a third selector for enabling the transmission FIFO circuit, and a fourth selector for enabling the reception FIFO circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 6,055,285 to Alston et al. teaches a FIFO circuit having synchronization signals to buffer data from one element to another.

US Patent No. 6,226,698 to Yeung et al. teaches a FIFO buffer to transfer data from a first circuit to a second circuit.

US Patent No. 5,982,772 to Oskouy teaches transmitting and receiving FIFOS having control signals indicating their status while transmitting data.

US Patent No. 4,463,443 to Frankel et al. teaches a FIFO to buffer data having a write and read signal generator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM

KIM HUYNH
SUPERVISORY PATENT EXAMINER

2/18/06